REMARKS/ARGUMENTS

This is in response to the Office Action mailed August 28, 2006, with claims 1-22 pending in the application. By this reply to the Office Action, claims 1, 14, and 17 have been amended. No new matter has been added. Claims 1-22 remain in consideration.

Claim Rejections 35 U.S.C. § 103(a)

Claims 1-12, 14, 17, and 20-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over applicant's Figure 1 in view of *Kato*, et al. USPN 5,548,601. Claims 13, 15, 16, 18, and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over applicant's Figure 1 in view of *Kato*, et al. '601 and further in view of *Weiberle*, et al. U.S. 2003/0006726 A1.

Claims 1, 14 and 17 have been amended to more particularly point out and distinctly claim the subject matter of the invention.

Claim 1 sets forth a brake control system, comprising, *inter alia*, a first supervisory controller, a second supervisory controller, and a monitoring controller operatively connected a controller bus and adapted to monitor the performance of said first supervisory controller, said second supervisory controller, said first brake control bus, and said second brake control bus. A brake actuation module has a direct signal line to each of the first and second supervisory controllers and the monitoring controller. Support for this claim language is found in the specification in Paras. 0015 and 0023.

Applicant respectfully asserts that the instant invention of newly amended claim 1 is patentably distinguishable from *Kato*, et al. and applicants' Figure 1 because all elements of the invention are NOT disclosed in the prior art, as required under 35 U.S.C. § 102 and §103(a). Specifically neither reference teaches or describes a brake actuation module having a direct signal line to each of the first and second supervisory controllers and the monitoring controller.

The office action cited *Kato*, et al. to teach the concept of a monitoring controller 80, 85. *Kato*, et al. teaches two control units CPU1 and CPU2 having dummy output terminals Td1 and Td2 which are input to a watchdog circuit 85 and a dummy output comparator 80 (*See*, Col. 6, Lines 46-55, and Fig. 5). The dummy output comparator 80 detects a failure in

the CPU1 and/or CPU2 when an exclusive OR circuit detects a disparity between the two dummy outputs. (*See*, Col. 7, Lines 27-33). The watchdog circuit 85 monitors processing times of the CPU1 and the CPU2. (*See*, Col. 7, Lines 40, et seq.). Neither the watchdog circuit nor the dummy output comparator of *Kato*, et al. include a brake actuation module having a direct signal line to each of a first and a second supervisory controller and a monitoring controller, as described above with respect to claim 1 of the instant invention.

Thus, newly amended claim 1 is distinguishable over the cited prior art, and therefore allowable.

Claim 14 sets forth a brake control system, comprising, *inter alia*, a first supervisory controller, a second supervisory controller, and a monitoring controller operatively connected a controller bus and adapted to monitor the performance of said first supervisory controller, said second supervisory controller, said first brake control bus, and said second brake control bus. The first and second supervisory controllers and the monitoring controller comprise substantially identically constructed control modules. Support for this claim language is found in the specification in Para. 0018.

The office action cited *Kato*, et al. to teach the concept of a monitoring controller 80, 85. *Kato*, et al. teaches two control units CPU1 and CPU2 having dummy output terminals Td1 and Td2 which are input to a watchdog circuit 85 and a dummy output comparator 80 (*See*, Col. 6, Lines 46-55, and Fig. 5). The dummy output comparator 80 detects a failure in the CPU1 and/or CPU2 when an exclusive OR circuit detects a disparity between the two dummy outputs. (*See*, Col. 7, Lines 27-33). The watchdog circuit 85 monitors processing times of the CPU1 and the CPU2. (*See*, Col. 7, Lines 40, et seq.). Neither the watchdog circuit nor the dummy output comparator of *Kato*, et al. comprises a control module that is substantially identical in construction to the CPU1 and the CPU2 as described above with respect to claim 14 of the instant invention.

Thus, newly amended claim 14 is distinguishable over the cited prior art, and therefore allowable.

Claim 17 sets forth a brake control system, comprising, *inter alia*, a first supervisory controller, a second supervisory controller, and a monitoring controller operatively connected a controller bus and adapted to monitor the performance of said first supervisory controller, said second supervisory controller, said first brake control bus, and said second brake control bus. A brake actuation module has a direct signal line to each of the first and second supervisory controllers and the monitoring controller, and, the first and second supervisory controllers and the monitoring controller comprise substantially identically constructed control modules.

Applicant respectfully asserts that the instant invention of newly amended claim 17 is patentably distinguishable from *Kato*, et al. and applicants' Figure 1 because all elements of the invention are NOT disclosed in the prior art, as required under 35 U.S.C. § 102 and §103(a).

The office action cited *Kato*, et al. to teach the concept of a monitoring controller 80, 85. *Kato*, et al. teaches two control units CPU1 and CPU2 having dummy output terminals Td1 and Td2 which are input to a watchdog circuit 85 and a dummy output comparator 80 (*See*, Col. 6, Lines 46-55, and Fig. 5). The dummy output comparator 80 detects a failure in the CPU1 and/or CPU2 when an exclusive OR circuit detects a disparity between the two dummy outputs. (*See*, Col. 7, Lines 27-33). The watchdog circuit 85 monitors processing times of the CPU1 and the CPU2. (*See*, Col. 7, Lines 40, et seq.). Neither the watchdog circuit nor the dummy output comparator of *Kato*, et al. include a brake actuation module having a direct signal line to each of a first and a second supervisory controller and a monitoring controller. Furthermore, neither the watchdog circuit nor the dummy output comparator of *Kato*, et al. comprises a control module that is substantially identical in construction to the CPU1 and the CPU2 as described above with respect to claim 17 of the instant invention.

Thus, newly amended claim 17 is distinguishable over the cited prior art, and therefore allowable.

Claims 2-12 and 20-22 all depend from one of independent claims 1, 14, or 17, and claim additional limitations thereto, and are therefore allowable.

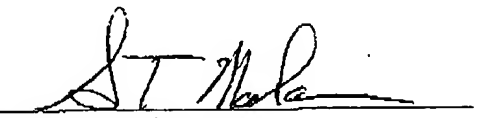
Claims 13, 15, 16, 18, and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over applicant's Figure 1 in view of *Kato*, et al. '601 and further in view of *Weiberle*, et al. U.S. 2003/0006726 A1.

Claims 13, 15, 16, 18, and 19 all depend from one of independent claims 1, 14, or 17, and claim additional limitations thereto, and are therefore allowable.

CONCLUSION

For at least all of the above, applicant respectfully requests reconsideration of claims 1-22, and requests withdrawal of any rejection of claims 1-22 based on applicants' Figure 1, *Kato*, et al. and *Weiberle*, et al. If the Examiner has any questions regarding the contents of the present response, the Applicants' attorney can be contacted at the telephone number appearing below.

Respectfully submitted,



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